Attorney Docket No.: 5649-951DV PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Jae-goo Lee
Serial No.: 10/756,543
Filed: January 13, 2004
For: INTEGRATED CIRCUIT MEMORY DEVICES

Group Art Unit No.: 2818
Examiner: David Nhu
Confirmation No.: 3863

Date: March 3, 2005

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION--37 C.F.R. § 41.37)

1. Transmitted herewith is the APPEAL BRIEF for the above-identified application, pursuant to the Notice of Appeal filed on January 6, 2005.

2. This application is filed on behalf of
☐ a small entity.

3. Pursuant to 37 C.F.R. § 41.20(b)(2), the fee for filing the Appeal Brief is:

☐	small entity	$250.00
☒	other than small entity	$500.00

Appeal Brief fee due $500.00

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Audra Wooten

AF #

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APPELLANT'S BRIEF ON APPEAL UNDER 37 C.F.R. §1.192

Sir:

This Appeal Brief is filed pursuant to the "Notice of Appeal to the Board of Patent Appeals and Interferences" mailed January 6, 2005.

Real Party In Interest

The real party in interest is assignee Samsung Electronics Co., Ltd., Republic of Korea.

Related Appeals and Interferences

To Appellant's knowledge, there are no currently pending appeals or interferences related to the present appeal.

Status of Claims

Claims 1-14 remain pending as of the filing date of this Brief. Each of these claims currently stands finally rejected. Appellant appeals the final rejection of Claims 1-14. The attached Appendix A presents the claims at issue as finally rejected in the Final Office Action of October 7, 2004 (hereinafter "Final Office Action").

Status of Amendments

The attached Appendix A presents the pending claims and each of the pending claims corresponding status. All amendments have been entered in the present case.

Summary of the Claimed Subject Matter

The present application includes Independent Claims 1, 6, and 8. Each of these claims is directed to an integrated circuit memory device. One embodiment of the present invention is shown in FIGS. 2C and 2D, below.

FIG. 2C of Present Application

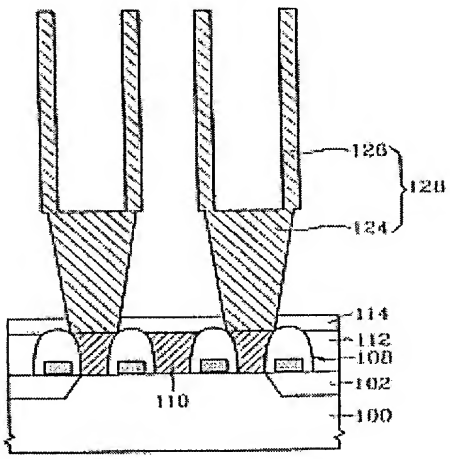
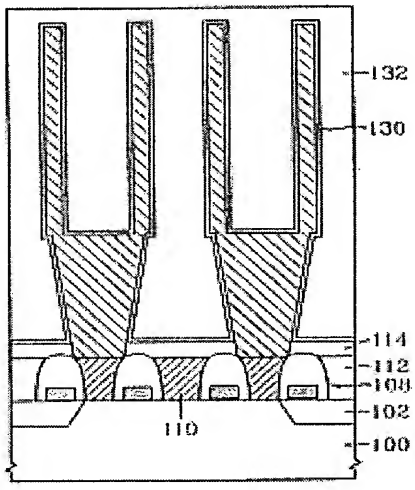


FIG. 2D of Present Application



The integrated circuit memory device includes a semiconductor substrate 100. A plurality of word line structures 108 are on the substrate 100. Word line contact plugs 110 are between adjacent word line structures 108. Storage node contact plugs 124 are in electrical contact with predetermines ones of the word line contact plugs 110. (Specification, page 8, lines 13-16). Storage node electrodes 126 are on the storage node contact plugs 124. (Specification, page 8, lines 16-20). As shown in FIG. 2C, an empty space is formed between sidewalls of both the storage node electrodes 126 and the storage node contact plugs 124. (Specification, page 8, line 23 to page 9, line 5). As shown in FIG. 2D, the empty space is filled with a plate electrode 132. (Specification, page 9, lines 8-13). The plate electrode 132 is thereby between the storage node electrodes 126 and between the storage node contact plugs 124.

Because the plate electrode 132 covers the sides of the storage node contact plugs 124 as well as the side of the storage node electrodes 126, the surface area of the lower electrodes 128 substantially increases. (Specification, page 9, lines 13-16). Consequently, even if the height of the lower electrodes 128 is not increased, the capacitance of a capacitor which is formed thereby may increase considerably. (Specification, page 9, lines 16-18).

Issue

Are Claims 1-14 properly rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent No. 6,555,481 to Nakamura (hereinafter " Nakamura")?

Argument

I. Introduction

Claims 1-14 are rejected under 35 U.S.C. § 102(e) as anticipated by Nakamura. Under 35 U.S.C. § 102, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." M.P.E.P. § 2131 (quoting *Verdegaal Bros. v. Union Oil Co.*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)). "Anticipation under 35 U.S.C. § 102 requires the disclosure in a single piece of prior art of each and every limitation of a claimed invention." *Apple Computer Inc. v. Articulate Sys. Inc.*, 57 U.S.P.Q.2d 1057, 1061 (Fed. Cir. 2000). "The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" M.P.E.P. § 2112 (citations omitted).

A finding of anticipation further requires that there must be no difference between the claimed invention and the disclosure of the cited reference as viewed by one of ordinary skill in the art. *See Scripps Clinic & Research Foundation v. Genentech Inc.*, 927 F.2d 1565, 1576, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). In particular, the Court of Appeals for the Federal Circuit held that a finding of anticipation requires absolute identity for each and every element set forth in the claimed invention. *See Trintec Indus. Inc. v. Top-U.S.A. Corp.*, 63 U.S.P.Q.2d 1597 (Fed. Cir. 2002). Additionally, the cited prior art reference must be enabling, thereby placing the allegedly disclosed matter in the possession of the public. *In re Brown*, 329 F.2d 1006, 1011, 141 U.S.P.Q. 245, 249 (C.C.P.A. 1964). Thus, the prior art reference must adequately describe the claimed invention so that a person of ordinary skill in the art could make and use the invention.

Appellant respectfully submits that the pending claims are patentable over the cited reference because the cited reference fails to disclose all of the recitations of the pending claims.

II. Independent Claims 1 and 8 Patentable Over Nakamura

Independent Claims 1 and 8 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nakamura. Appellant respectfully submits that many of the recitations of these claims are not disclosed by Nakamura.

Independent Claim 1 recites (emphasis added):

> 1. An integrated circuit memory device comprising:
> a semiconductor substrate;
> a plurality of word line structures on predetermined portions of the semiconductor substrate;
> word line contact plugs, each of which is disposed between adjacent word line structures;
> storage node contact plugs in electrical contact with predetermined ones of the word line contact plugs;
> storage node electrodes on the storage node contact plugs; and
> a plate electrode between the storage node electrodes and between the storage node contact plugs.

Accordingly, storage node contact plugs are in electrical contact with word line contact plugs, storage node electrodes are on the storage node contact plugs, and the plate electrode is between the storage node electrodes and between the storage node contact plugs. In rejecting Claim 1, the Final Office Action states on page 2 that Nakamura discloses "storage node contact plugs 14, SNC in electrical contact with predetermined ones of the [word line] WL contact plugs; storage node electrodes 16 on the storage node contact plugs; and plate electrodes 18 between the storage node electrodes and between the storage node contact plugs 14, SNC (see figures 9A-9B)." However, this interpretation of Nakamura by the Final Office Action appears to be contrary to the referenced figures and discussion of Nakamura.

Initially, Appellant notes that the Final Office Action has advanced a new interpretation of Nakamura that is different from that made in the Office Action dated May 11, 2004, and which was first raised in the Final Office Action. The Office Action dated May 11, 2004 had contended on Page 2 that bit line 11 discloses a "storage node contact plug". The Final Office Action appears to no longer make that contention, and instead now contends

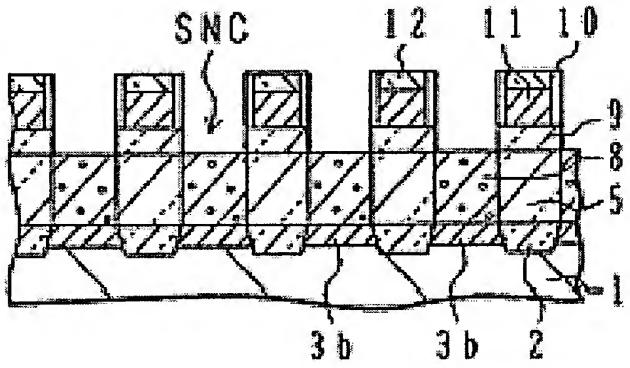
that the storage electrode plug 14 that is formed in the storage node opening (SNC) is a storage node contact plug as recited in Claim 1. The Final Office Action now contends that Nakamura teaches "storage node contact plugs 14, SNC (see figures 9A-9B); a plate electrode 18 on the dielectric layer 5, 9 and between the storage node contact plugs and between the storage node electrodes 16, 18". (Final Office Action, Pages 4-5).

Nakamura discloses the following process for forming the structure that is referenced by the Final Office Action to reject Claim 1:

> As shown in FIGS. 8A to 8D, by using the etch stopper film 12 as a mask, the exposed second interlayer insulating film 9 is anisotropically etched. This anisotropic etching forms a storage node opening SNC exposing the lower plug 8. The storage node opening SNC can be formed by using the mask for defining the bit line contact area and an additional mask is not necessary.

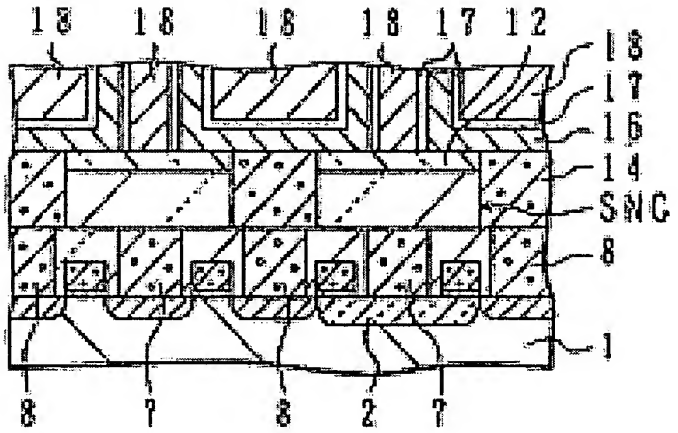
(Nakamura, Col. 8, lines 13-19). The resultant structure is shown below in FIG. 8D of Nakamura in which the storage node opening SNC is formed in each area that was not masked by the etch stopper film 12.

FIG.8D



Nakamura then explains that, "as shown in FIGS. 9A to 9D, a storage electrode plug 14 is formed in the storage node opening SNC ... [by] forming a polysilicon layer over the whole substrate surface and removing the polysilicon layer at the level higher than the surface of the etch stopper film 12 by CMP or the like. " (Nakamura, Col. 8, lines 20-26, emphasis added). The resultant structure is shown below in FIG. 9B of Nakamura.

FIG.9B



Nakamura then explains that a storage electrode 16 and a plate electrode 18 are formed as follows:

> Thereafter, a storage capacitor is formed on the storage electrode plug 14 by a known method. For example, the storage capacitor is formed in the following manner. A sacrificial film of silicon oxide or the like is first formed, and an opening for the storage electrode is formed. A storage electrode 16 is formed on the inner surface of the storage electrode opening, for example, by depositing an Ru film. After the storage electrode film on the sacrificial film is removed, the sacrificial film is removed. A capacitor dielectric film 17 is formed on the whole substrate surface, and a plate electrode 18 is formed thereon.
>
> (Nakamura, Col. 8, lines 26-36).

As shown in FIG. 9B and explained in Nakamura, a top surface of etch stopper film 12 is aligned with and extends between the top surface of the storage electrode plugs 14 to form a resultant planar surface. The storage electrode 16 and plate electrode 18 are formed on that resultant planar surface. Consequently, although the plate electrode 18 is between the storage electrodes 16, it is not, and cannot be, between the storage electrode plug 14 because the etch stopper film 12 prevents any such subsequently formed structure from extending down to between the storage electrode plugs 14.

In sharp contrast to Nakamura, an embodiment of the present invention that is shown below in FIG. 2C from the present application illustrates that an empty space is formed between sidewalls of both the storage node electrodes 126 and the storage node contact plugs 124. That empty space is then filled with the plate electrode 132, so that the plate electrode

132 is between the storage node electrodes 126 and between the storage node contact plugs 124, as shown in FIG. 2D below.

FIG. 2C of Present Application

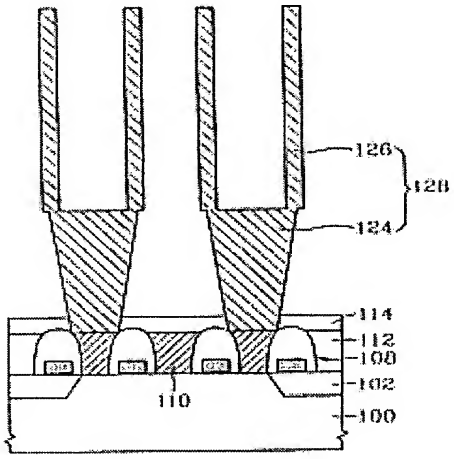
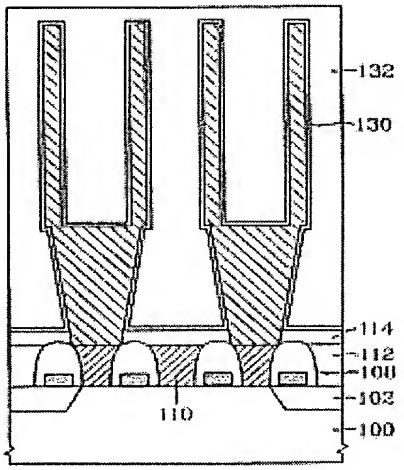


FIG. 2D of Present Application



According to the legal standard for anticipation set out above, **each and every element** as set forth in the claim must be found in Nakamura. Furthermore, that there must be **no difference** between the claimed invention and the disclosure of Nakamura. As discussed above, there are many differences between Nakamura and Independent Claim 1. In particular, the plate electrode 18 of Nakamura is not between the storage electrode plug 14.

Independent Claim 8 recites, among other things, "a plate electrode on the dielectric layer and between the storage node contact plugs and between the storage node electrodes." Accordingly, Claim 8 is patentable over Nakamura for substantially at least the same reasons as explained for Claim 1.

Accordingly, Appellants respectfully submit that Independent Claims 1 and 8 are not anticipated by Nakamura for at least the reasons discussed above. Thus, independent Claims 1 and 8 are patentable over Nakamura. Furthermore, dependent Claims 3-5 and 12-14 are patentable at least per the patentability of independent base Claims 1 and 8 from which they depend. Accordingly, Appellants respectfully request reversal of the rejections with respect to Claims 1 and 8 and the claims that depend therefrom for at least the reasons discussed herein.

III. Claims 2 and 9 are Patentable Over Nakamura

Claims 2 and 9 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nakamura. Claims 2 and 9 depend from independent Claims 1 and 8, respectively, and thus are patentable over Nakamura based on the reasons discussed above for Claims 1 and 8. In addition, Appellant respectfully submits that Claims 2 and 9 are also patentable over Nakamura for at least one additional independent reason.

In particular, Claims 2 and 9 each recites that the plate electrode extends between lower portions of the storage node contact plugs. The Final Office Action summarily rejects Claim 2 on the basis that "Nakamura, col. 1-14, also teach wherein the plate electrode extends between lower portions of the storage node contact plugs (see figures 22A-22D)." (Final Office Action, Page 2). The Final Office Action does not explain what elements of FIGS. 22A-D or particular description of Nakamura supports such contention.

Figures 22A-D of Nakamura are shown below.

FIG.22A

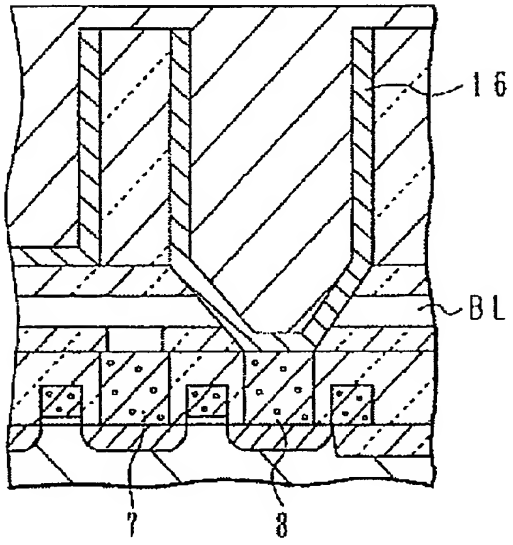


FIG.22B

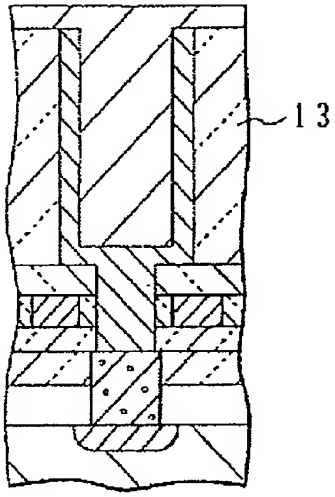


FIG.22C

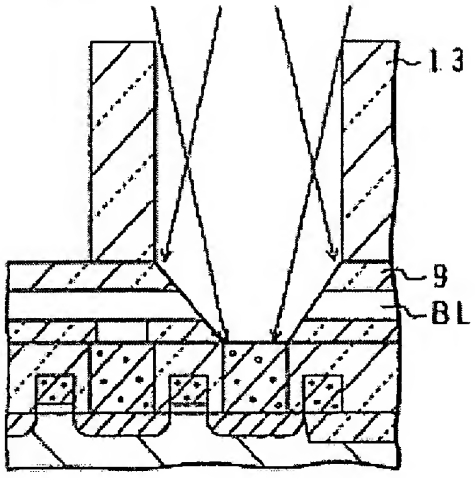
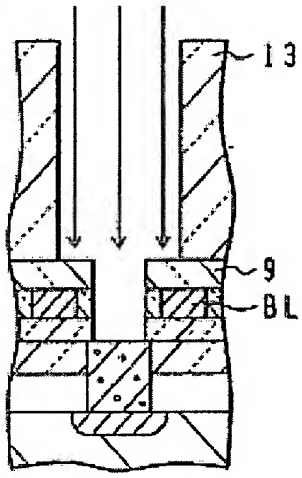


FIG.22D



Initially, Appellant notes that Nakamura describes FIGS 6-9 as illustrating one embodiment of a semiconductor device, and FIGS. 22A-D as illustrating a different embodiment of a semiconductor device. (See Nakamura, Col. 4, lines 7-10 and 25-29). Accordingly, FIGS. 22A-D are interpreted based on the corresponding description in Nakamura from Col. 11, line 8 to Col. 13, line 4. Nakamura describes that FIGS. 22A-D illustrate an example shape of a storage electrode 16 that extends through an insulating film 13 and a bit line (BL), and to connect with a lower plug 8. Nakamura describes and shows a single storage electrode 16. Again, the Final Office Action does not explain what elements of FIGS. 22A-D or particular description of Nakamura supports the content that FIGS. 22A-D disclose a "plate electrode [that] extends between lower portions of the storage node contact plugs". If the lower plug 8 is construed to be the word line contact plug in Claim 1, and the storage electrode 16 is construed to be the "storage node electrode", then Nakamura would still fail to disclose a storage node electrode on the storage node contact plug, is would also fail to disclose any plate electrode whatsoever. Moreover, it fails to disclose a plate electrode that extends between a lower portion of a storage node contact plug, as claimed by each of Claims 2 and 9.

Accordingly, Appellant respectfully submits that the rejections of Claims 2 and 9 should be reversed.

IV. Claim 11 is Patentable Over Nakamura

Claim 11 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Nakamura. Claim 11 depends from independent Claim 8, and thus is patentable over Nakamura based on the same reasons discussed above for Claim 8. In addition, Appellant respectfully submits that Claim 11 is also patentable over Nakamura for at least one additional independent reason.

Claim 11 recites:

> 11. (Original) The integrated circuit memory device of claim 8, wherein the storage node contact plugs are directly on the bit line structures.

Accordingly, the storage node contact plugs are directly on the bit line structures. Although the Office Action dated May 11, 2004 and the Final Office Action have rejected Claim 9 over Nakamura, neither of these Actions has contended that Nakamura discloses storage node contact plugs that are directly on a bit line structure. Appellant identified on Page 8 of the Amendment dated July 29, 2004 that the Office Action dated May 11, 2004 failed to disclose where Nakamura discloses the recitation of Claim 11. However, the Final Office Action continued to reject Claim 11 over Nakamura without providing any basis for that rejection. Appellant suggests that Nakamura does not disclose the recitations of Claim 11. Accordingly, Appellant respectfully submits that the rejections of Claim 11 should be reversed.

V. Independent Claim 6 is Patentable Over Nakamura

Independent Claim 6 and dependent Claim 7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nakamura. Appellant respectfully submits that many of the recitations of these claims are not disclosed by Nakamura.

Independent Claim 6 recites (emphasis added):

> 6. An integrated circuit memory device, comprising:
> a semiconductor substrate;
> a pair of spaced apart word line structures on the substrate;
> an interlayer insulating layer on the word line structures;
> a bit line structure on the interlayer insulating layer that is transverse to the word line structures;
> a first capacitor electrode that extends from the substrate between adjacent word line structures, through the interlayer insulation layer, and beyond the bit line structure;
> a capacitor dielectric on the first capacitor electrode and directly on the bit line structure; and

a second capacitor electrode on the capacitor dielectric.

Accordingly, Claim 6 recites that the capacitor dielectric is directly on the bit line structure, and the second capacitor electrode in on the capacitor dielectric. In rejecting Claim 6, the Office Action contends that Nakamura discloses "a capacitor dielectric 17 on the first capacitor electrode and directly on the BL structures", where the first capacitor electrode is referred to as element 16 and the BL structure is referred to as element 11. However, this contention is not supported by the disclosure of Nakamura, which shows in FIGs. 19A-D that the capacitor dielectric 17 is not directly on the bit line 11. Instead, FIGs. 19A and 19C shows intervening elements 13 and 12, and FIG. 19D shows intervening elements 16 and 12. FIGs. 19A-D of Nakamura are shown below for convenience.

FIG.19A

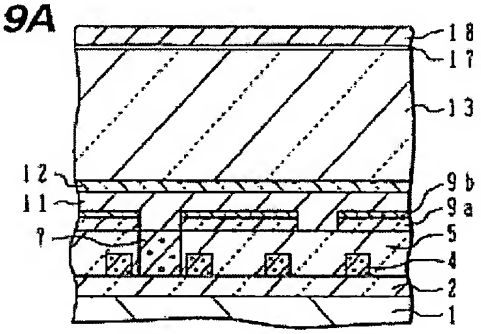


FIG.19B

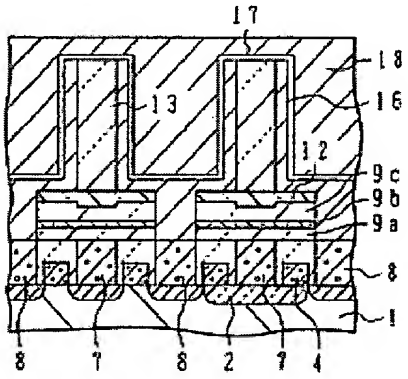


FIG.19C

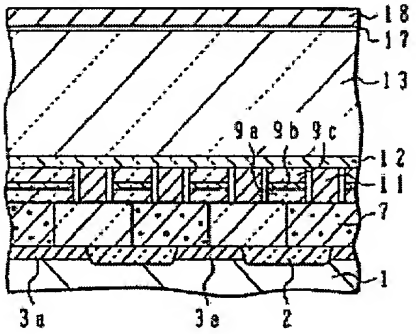
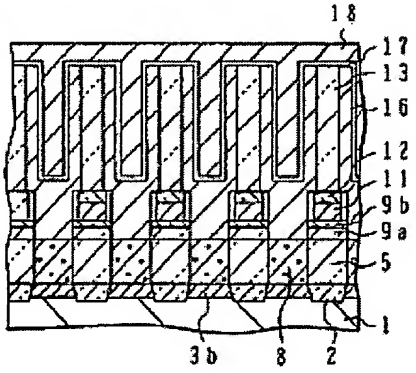


FIG.19D



For at least these reasons, Appellant respectfully submits that Nakamura fails to disclose each and every element of Claim 6, and therefore that Claim 6 is patentable over Nakamura.

Claim 7 is patentable at least one the basis that it depends from patentable Claim 6.

Accordingly, Appellant respectfully submits that the rejections of Claims 6 and 7 should be reversed.

VI. Conclusion

In light of the above discussion, Appellant submits that each of the pending claims is patentable over the cited references and, therefore, requests reversal of the rejections of Claims 1-14 and passing of the application to issue.

It is not believed that an extension of time and/or additional fee(s) are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned for under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to Deposit Account No. 09-0461.

Respectfully submitted,

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Audra Wooten

APPENDIX A
Pending Claims USSN 10/756,543
Filed January 13, 2004

1. (Original) An integrated circuit memory device comprising:

a semiconductor substrate;

a plurality of word line structures on predetermined portions of the semiconductor substrate;

word line contact plugs, each of which is disposed between adjacent word line structures;

storage node contact plugs in electrical contact with predetermined ones of the word line contact plugs;

storage node electrodes on the storage node contact plugs; and

a plate electrode between the storage node electrodes and between the storage node contact plugs.

2. (Original) The integrated circuit memory device of claim 1, wherein the plate electrode extends between lower portions of the storage node contact plugs.

3. (Original) The integrated circuit memory device of claim 1, further comprising a plate insulating layer between the plate electrode and the storage node contact plugs that insulates the plate electrode from the storage node contact plugs.

4. (Original) The integrated circuit memory device of claim 1, wherein the storage node electrodes are directly on the storage node contact plugs.

5. (Original) The integrated circuit memory device of claim 1, wherein the word line structures each comprise a gate electrode, a gate insulating layer insulating the gate electrode from the semiconductor substrate, and an insulating material covering a top surface and sides of the gate electrode.

6. (Original) An integrated circuit memory device, comprising:

a semiconductor substrate;

a pair of spaced apart word line structures on the substrate;

an interlayer insulating layer on the word line structures;

a bit line structure on the interlayer insulating layer that is transverse to the word line structures;

a first capacitor electrode that extends from the substrate between adjacent word line structures, through the interlayer insulation layer, and beyond the bit line structure;

a capacitor dielectric on the first capacitor electrode and directly on the bit line structure; and

a second capacitor electrode on the capacitor dielectric.

7. (Original) The memory device according to Claim 6, wherein the capacitor dielectric is directly on the interlayer insulation layer.

8. (Original) An integrated circuit memory device comprising:

a semiconductor substrate;

a plurality of word line structures on predetermined portions of the semiconductor substrate;

word line contact plugs between adjacent word line structures;

bit line structures in electrical contact with a first set of the word line contact plugs;

storage node contact plugs on, and electrically connected to, a second set of the word line contact plugs that is different from the first set of the word line contact plugs;

storage node electrodes on the storage node contact plugs;

a dielectric layer on the storage node contact plugs and the storage node electrodes; and

a plate electrode on the dielectric layer and between the storage node contact plugs and between the storage node electrodes.

9. (Original) The integrated circuit memory device of claim 8, wherein the plate electrode is between lower portions of the storage node contact plugs.

10. (Original) The integrated circuit memory device of claim 8, wherein the storage node contact plugs are directly on the second set of the word line contact plugs.

11. (Original) The integrated circuit memory device of claim 8, wherein the storage node contact plugs are directly on the bit line structures.

12. (Original) The integrated circuit memory device of claim 8, wherein the storage node electrodes are directly on the storage node contact plugs.

13. (Previously presented) ~~the~~ The integrated circuit memory device of claim 8, wherein the dielectric layer is directly on the bit line structures.

14. (Original) The integrated circuit memory device of claim 8, wherein:

the word line structures each comprise a gate electrode, a gate insulating layer which insulates the gate electrode from the semiconductor substrate, and an insulating material on a top surface and sides of the gate electrode, and

the bit line structures each comprise a bit line and a dielectric layer on a top surface and sides of the bit line.